CLAIMS

What is claimed is:

1. A low voltage, 5V tolerant buffer, comprising:

a series connection of at least three transistors, a terminal of an upper transistor in said series connection being connected to a PAD, and a terminal of a lower transistor of said series connection being connected to ground; and

a bias generator, an output of said bias generator being connected to a gate of said upper transistor;

wherein a gate of a central one of said series connection of three transistors is adapted to be connected to a power supply of no greater than 2.5V nominal.

2. The low voltage, 5V tolerant buffer according to claim 1, wherein said bias generator comprises:

a series connection of two p-channel field effect transistors;

said series connection of said two transistors being connected between said power supply and said ground.

3. The low voltage, 5V tolerant buffer according to claim 2, wherein:

a gate of one of said two transistors is adapted to be coupled to said PAD, and a gate of the other of said two transistors is adapted to be driven by said power supply.

4. The low voltage, 5V tolerant buffer according to claim 1, wherein:

said upper transistor, said lower transistor, and said central transistor are each an n-channel field effect transistor.

5. The low voltage, 5V tolerant buffer according to claim 1, wherein:

said buffer can reliably sink no more than about 16 milliamps of current.

6. The low voltage, 5V tolerant buffer according to claim 1, wherein:

said buffer is comprised in a SCSI bus.

7. The low voltage, 5V tolerant buffer according to claim 1, wherein:

said buffer is comprised in a PCI bus.

8. The low voltage, 5V tolerant buffer according to claim 1, wherein:

said buffer is comprised in a PCMCIA bus.

9. The low voltage, 5V tolerant buffer according to claim 1, further comprising:

an input stage driven by a node between said central transistor and said lower transistor;

wherein said buffer is a bi-directional buffer.

10. The low voltage, 5V tolerant buffer according to claim 1, further comprising:

an integrated circuit including said 5V tolerant buffer.

11. The low voltage, 5V tolerant buffer according to claim 1, wherein:

a channel width of at least one of said at least three transistors is at least 400 um.

12. The low voltage, 5V tolerant buffer according to claim 1, wherein:

said series connection of at least three transistors is a series connection of a current path of each of said at least three transistors.

13. The low voltage, 5V tolerant buffer according to claim 1, wherein:

each of said at least three transistors are a field effect transistor.

14. A method of providing a low voltage, 5V tolerant buffer, comprising:

providing a series connection of at least three transistors;

connecting an end of an upper transistor in said series connection to a PAD;

connecting an end of a lower transistor of said series connection to ground;

providing a bias voltage to a gate of said upper transistor, said bias voltage being based on a difference between a power supply voltage and a voltage at said PAD; and

providing a power supply input to a gate of a central one of said series connection of three transistors.

15. The method of providing a low voltage, 5V tolerant buffer according to claim 14, further comprising:

providing a power supply voltage of no greater than 2.5V nominal.

16. The method or providing a low voltage, 5V tolerant buffer according to claim 14, further comprising:

providing a power supply voltage of no greater than 2.0V nominal.

17. The method of providing a low voltage, 5V tolerant buffer according to claim 14, further comprising:

providing a power supply voltage of no greater than 1.8V nominal.

18. The method of providing a low voltage, 5V tolerant buffer according to claim 14, further comprising:

providing an input stage adapted to be driven by a node between said central transistor and said lower transistor.

19. The method of providing a low voltage, 5V tolerant buffer according to claim 14, wherein:

said buffer is comprised in a SCSI bus.

20. Apparatus for providing a low voltage, 5V tolerant buffer, comprising:

means for inverting an input signal;

means for connecting a terminal of an upper transistor in said series connection to a PAD;

means for connecting a terminal of a lower transistor of said series connection to ground;

means for providing a bias voltage to a gate of said upper transistor, said bias voltage being based on a difference between a power supply voltage and a voltage at said PAD; and

means for coupling a power supply input to a gate of a central one of said series connection of three transistors.

21. The apparatus for providing a low voltage, 5V tolerant buffer according to claim 20, further comprising:

means for providing a power supply voltage of no greater than 2.5V nominal.

22. The apparatus for providing a low voltage, 5V tolerant buffer according to claim 20, further comprising:

means for coupling a power supply voltage of no greater than 2.0V nominal.

23. The apparatus for providing a low voltage, 5V tolerant buffer according to claim 20, further comprising:

means for providing a power supply voltage of no greater than 1.8V nominal.

24. The apparatus for providing a low voltage, 5V tolerant buffer according to claim 20, further comprising:

means for providing an input stage adapted to be driven by a node between a central transistor and said lower transistor;

wherein said buffer is a bi-directional buffer.

25. The apparatus for providing a low voltage, 5V tolerant buffer according to claim 20, wherein:

said buffer is comprised in a SCSI bus.